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1 Reducing wire delay penalty through value prediction
Joan-Manuel Parcerisa, Antonio González
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**
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2 Latency and latch count minimization in wave steered circuits
Amit Singh, Arindam Mukherjee, Malgorzata Marek-Sadowska
June 2001 **Proceedings of the 38th conference on Design automation**
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Wave Steering is a new design methodology that realizes high throughput circuits by embedding layout friendly synthesized structures in silicon. Wave Steered circuits inherently utilize latches in order to guarantee the correct signal arrival times at the inputs of these synthesized structures and maintain the high throughput of operation. In this paper, we show a method of reor-dering signals to achieve minimum circuit latency for Wave Steered circuits and propose an Integer Linear Program ...

3 Emerging areas: Fault-tolerant platforms for automotive safety-critical applications
M. Baleani, A. Ferrari, L. Mangeruca, A. Sangiovanni-Vincentelli, Maurizio Peri, Saverio Pezzini
October 2003 **Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems**
Full text available: pdf(736.40 KB)
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Fault-tolerant electronic sub-systems are becoming a standard requirement in the automotive industrial sector as electronics becomes pervasive in present cars. We address the issue of fault tolerant chip architectures for automotive applications. We begin by reviewing fault-tolerant architectures commonly used in other industrial domains where fault-tolerant electronics has been a must for a number of years, e.g., the aircraft manufacturing industrial sector. We then proceed to investigate how t ...

Keywords: VLSI, automotive, fault-tolerant, multi-processor, safety critical, system-on-a-